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**1 [Hardware/software co-design of a fuzzy RISC processor](#)**

V. Salapura, M. Gschwind

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

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**Keywords:** hardware/software co-evaluation, hardware/software co-design, processor core, MIPS RISC processor, fuzzy processing, fuzzy rule evaluation, application specific instruction set processor (ASIP), subword parallelism, VHDL, logic synthesis, instruction set definition, instruction set architecture, performance evaluation

**2 [Fast Prolog with an extended general purpose architecture](#)**

Bruce K. Holmer, Barton Sano, Michael Carlton, Peter Van Roy, Ralph Haygood, William R. Bush, Alvin M. Despain, Joan M. Pendleton, Tep Dobry

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture**, Volume 18 Issue 3

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**3 [The PL/EXUS language and virtual machine](#)**

Gary A. Sitton, Thomas A. Kendrick, A. Gil Carrick

November 1973 **ACM SIGPLAN Notices , Proceedings of a symposium on High-level-language computer architecture**, Volume 8 Issue 11

Full text available:  pdf(640.09 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

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S. Abe, T. Bandoh, S. Yamaguchi, K. Kurosawa, K. Kiriyaama





June 1987 **Proceedings of the 14th annual international symposium on Computer architecture**

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